**LAB 2**

**UNIVERSAL LOGIC GATES**

**Note: Make sure to give proper headings (as the one mentioned below) for each gate while making this lab report**

**Task 1**

Simulate the logic gates (NOT, AND, OR, NOR, Ex-OR, Ex-NOR) using only NAND gates in Logicly software.

Make a truth table and verify all the combinations for each of these gates. Paste the screenshots of your circuit (logic diagram) for each of above mentioned gates having all the combinations. For example, if you make a NOT gate using NAND gate, simulate it for both of its possible combinations i.e. 0 and 1 and paste its screenshot (for both combinations).

**NOT using NAND Gate**

**Task 2**

**Simulate the logic gates (NOT, AND, NAND, OR, Ex-OR, Ex-NOR) using only NOR gates in Logicly software.**

**Make a truth table and verify all the combinations for each of these gates. Paste the screenshots of your circuit (logic diagram) for each of above mentioned gates having all the combinations. For example, if you make a NOT gate using NOR gate, simulate it for both of its possible combinations i.e. 0 and 1 and paste its screenshot (for both combinations).**